AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0001] with the following:

This application claims the benefit of U.S. Provisional Application No. 60/252,724 entitled "METHOD AND APPARATUS FOR STORAGE I/O WITH FULL-DUPLEX ONE-TIME BLOCK I/O TRANSFER AND ADAPTIVE PAYLOAD SIZING," filed November 22, 2000, and is related to U.S. Patent Application No. 10/037,168 entitled "METHOD AND SYSTEM FOR PLESIOSYNCHRONOUS COMMUNICATIONS WITH NULL INSERTION AND REMOVAL"; U.S. Patent Application No. 10/045,393, entitled "METHOD AND SYSTEM FOR TRANSITION-CONTROLLED SELECTIVE BLOCK INVERSION COMMUNICATIONS"; U.S. Patent Application No. 10/035,591 entitled "COMMUNICATIONS ARCHITECTURE FOR STORAGE-BASED DEVICES"; U.S. Patent Application No. 10/036,591 entitled "METHOD AND SYSTEM FOR PACKET ORDERING BASED ON PACKET TYPE"; U.S. Patent Application No. 10/036,794 entitled "METHOD AND SYSTEM FOR HOST HANDLING OF COMMUNICATIONS ERRORS"; U.S. Patent Application No. 10/045,606 entitled "METHOD AND SYSTEM FOR DYNAMIC SEGMENTATION OF COMMUNICATIONS PACKETS"; U.S. Patent Application No. 10/045,348 entitled "METHOD AND SYSTEM FOR ASYMMETRIC PACKET ORDERING BETWEEN COMMUNICATIONS DEVICES"; U.S. Patent Application No. 10/053,461 entitled "METHOD AND SYSTEM FOR COMMUNICATING CONTROL INFORMATION VIA OUT-OF-BAND SYMBOLS"; U.S. Patent Application No. 10/045,625 entitled "METHOD AND SYSTEM FOR INTEGRATING PACKET TYPE INFORMATION WITH SYNCHRONIZATION SYMBOLS"; U.S. Patent Application No. 10/035,911 entitled "METHOD AND SYSTEM FOR NESTING OF COMMUNICATIONS PACKETS"; U.S. Patent Application No. 10/045,297 entitled "COMMUNICATIONS ARCHITECTURE FOR MEMORY-BASED DEVICES"; U.S. Patent Application No. 10/045,600 entitled "METHOD AND SYSTEM FOR DC-BALANCING AT THE PHYSICAL LAYER"; and U.S. Patent Application No. 10/045,601 entitled "MULTISECTION MEMORY BANK SYSTEM", which are all hereby incorporated by reference in their entirety.